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L3	16476	interrupt$3 same priority	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/14 11:02
L4	786	page adj2 miss	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/14 11:02
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L6	68	((empty or open) near2 page) and (interrupt$3 same priority)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/14 11:02
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L13	12104	11 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/14 11:02
L14	68	2 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/14 11:02
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#1	((memory arbitration<in>metadata) <and> (interrupt request<in>metadata)) <and> (priority<in>metadata)
#2	((memory arbitration<in>metadata) <and> (interrupt request<in>metadata)) <and> (priority<in>metadata)
#3	page miss
#4	(empty page<IN>metadata)
#5	open page
#6	(plurality counter<IN>metadata)
#7	plurality counters
#8	#2 and #3
#9	(mmu and arbitration<in>metadata)
#10	#8 and #4
#11	#8 and #10

[redacted]

Terms used
arbitration memory arbiter priority interrupt request counter lower priority scheduler

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1 Experience Using Multiprocessor Systems—A Status Report

Anita K. Jones, Peter Schwarz

June 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 2

Publisher: ACM Press

Full text available: pdf(4.48 MB) Additional Information: full citation, references, citings, index terms

2 The minerva multi-microprocessor

Lawrence C. Widdoes

January 1976 **ACM SIGARCH Computer Architecture News , Proceedings of the 3rd annual symposium on Computer architecture ISCA '76**, Volume 4 Issue 4

Publisher: ACM Press

Full text available: pdf(651.29 KB) Additional Information: full citation, abstract, references, citings, index terms

A multiprocessor system is described which is an experiment in low cost, extensible, multiprocessor architectures. Global issues such as inclusion of a central bus, design of the bus arbiter, and methods of interrupt handling are considered. The system initially includes two processor types, based on microprocessors, and these are discussed. Methods for reducing processor demand for the central bus are described.

3 A VLIW architecture for a trace scheduling compiler

Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman

October 1987 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the second international conference on Architectual support for programming languages and operating systems ASPLOS-II**, Volume 15 , 22 , 21 Issue 5 , 10 , 4

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.59 MB) Additional Information: full citation, abstract, references, citings, index terms

Very Long Instruction Word (VLIW) architectures were promised to deliver far more than the factor of two or three that current architectures achieve from overlapped execution. Using a new type of compiler which compacts ordinary sequential code into long instruction words, a VLIW machine was expected to provide from ten to thirty times the performance of a more conventional machine built of the same implementation technology.Multiflow Computer, Inc., has now built a VLIW called the TRACE™< ...

4 High level and architectural synthesis: Round-robin arbiter design and generation

Eung S. Shin, Vincent J. Mooney, George F. Riley
October 2002 **Proceedings of the 15th international symposium on System Synthesis**
Publisher: ACM Press
Full text available: pdf(232.92 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we introduce a Round-robin Arbiter Generator (RAG) tool. The RAG tool can generate a design for a Bus Arbiter (BA). The BA is able to handle the exact number of bus masters for both on-chip and off-chip buses. RAG can also generate a distributed and parallel hierarchical Switch Arbiter (SA). The first contribution of this paper is the automated generation of a round-robin token passing BA to reduce time spent on arbiter design. The generated arbiter is fair, fast, and has a low an ...

Keywords: arbiter, distributed arbiter, round-robin token passing, synthesis, terabit switch

5 Concert: design of a multiprocessor development system

R. R. Halstead, T. L. Anderson, R. B. Osborne, T. L. Sterling
June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture ISCA '86**, Volume 14 Issue 2
Publisher: IEEE Computer Society Press, ACM Press
Full text available: pdf(773.95 KB) Additional Information: full citation, abstract, references, citings, index terms

Concert is a shared-memory multiprocessor testbed intended to facilitate experimentation with parallel programs and programming languages. It consists of up to eight clusters, with 4-8 processors in each cluster. The processors in each cluster communicate using a shared bus, but each processor also has a private path to some memory. The novel feature of Concert is the RingBus, a segmented bus in the shape of a ring that permits communication between cluster ...

6 A SMART scheduler for multimedia applications

Jason Nieh, Monica S. Lam
May 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 2
Publisher: ACM Press
Full text available: pdf(570.87 KB) Additional Information: full citation, abstract, references, index terms

Real-time applications such as multimedia audio and video are increasingly populating the workstation desktop. To support the execution of these applications in conjunction with traditional non-real-time applications, we have created SMART, a Scheduler for Multimedia And Real-Time applications. SMART supports applications with time constraints, and provides dynamic feedback to applications to allow them to adapt to the current load. In addition, the support for real-time applications is integrat ...

Keywords: Scheduling, multimedia, proportional sharing, real-time

7 The SGI Origin: a ccNUMA highly scalable server

James Laudon, Daniel Lenoski
May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture ISCA '97**, Volume 25 Issue 2
Publisher: ACM Press
Additional Information: full citation, abstract, references, citings, index

Full text available: pdf(1.74 MB) terms

The SGI Origin 2000 is a cache-coherent non-uniform memory access (ccNUMA) multiprocessor designed and manufactured by Silicon Graphics, Inc. The Origin system was designed from the ground up as a multiprocessor capable of scaling to both small and large processor counts without any bandwidth, latency, or cost cliffs. The Origin system consists of up to 512 nodes interconnected by a scalable Craylink network. Each node consists of one or two R10000 processors, up to 4 GB of coherent memory, and ...

8 Preventing interrupt overload

John Regehr, Usit Duongsaa

June 2005 **ACM SIGPLAN Notices , Proceedings of the 2005 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems LCTES'05**, Volume 40 Issue 7

Publisher: ACM Press

Full text available: pdf(291.66 KB) Additional Information: full citation, abstract, references, index terms

Performance guarantees can be given to tasks in an embedded system by ensuring that access to each shared resource is mediated by an appropriate scheduler. However, almost all previous work on CPU scheduling has focused on thread-level scheduling, resulting in systems that are vulnerable to a lower-level form of overload that occurs when too many interrupts arrive. This paper describes three new techniques, two software-based and one hardware-based, for creating systems that delay or drop excess ...

Keywords: embedded, interrupts, overload, scheduling

9 VLSI assist for a multiprocessor

Bob Beck, Bob Kasten, Shreekant Thakkar

October 1987 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the second international conference on Architectual support for programming languages and operating systems ASPLOS-II**, Volume 15 , 22 , 21 Issue 5 , 10 , 4

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, references, citings, index terms

Multiprocessors have long been of interest to computer community. They provide the potential for accelerating applications through parallelism and increased throughput for large multi-user system. Three factors have limited the commercial success of multiprocessor systems; entry cost, range of performance, and ease of application. Advances in very large scale integration (VLSI) and in computer aided design (CAD) have removed these limitations, making possible a new class of multiprocessor system ...

10 A survey of commercial parallel processors

Edward Gehringer, Janne Abullarade, Michael H. Gulyn

September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4

Publisher: ACM Press

Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

11 Improving interactive performance using TIPME

Yasuhiro Endo, Margo Seltzer
June 2000 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2000 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '00**, Volume 28 Issue 1
Publisher: ACM Press

Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, citings, index terms

On the vast majority of today's computers, the dominant form of computation is GUI-based user interaction. In such an environment, the user's perception is the final arbiter of performance. Human-factors research shows that a user's perception of performance is affected by unexpectedly long delays. However, most performance-tuning techniques currently rely on throughput-sensitive benchmarks. While these techniques improve the average performance of the system, they do littl ...

Keywords: interactive performance, monitoring

12 Towards a taxonomy of software connectors

Nikunj R. Mehta, Nenad Medvidovic, Sandeep Phadke
June 2000 **Proceedings of the 22nd international conference on Software engineering**
Publisher: ACM Press

Full text available: pdf(184.27 KB) Additional Information: full citation, abstract, references, citings, index terms

Software systems of today are frequently composed from prefabricated, heterogeneous components that provide complex functionality and engage in complex interactions. Existing research on component-based development has mostly focused on component structure, interfaces, and functionality. Recently, software architecture has emerged as an area that also places significant importance on component interactions, embodied in the notion of software connectors. However, the current level of underst ...

Keywords: classification, software architecture, software connector, taxonomy

13 Priority-driven, preemptive I/O controllers for real-time systems

B. Sprunt, D. Kirk, L. Sha
May 1988 **ACM SIGARCH Computer Architecture News , Proceedings of the 15th Annual International Symposium on Computer architecture ISCA '88**, Volume 16 Issue 2
Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.00 MB) Additional Information: full citation, abstract, references, index terms

Current I/O controller architectures inhibit the use of priority-driven preemptive scheduling algorithms that can guarantee hard deadlines in real-time systems. This paper examines the effect of three I/O controller architectures upon schedulable utilization, which is the highest attainable resource utilization at or below which all deadlines can be guaranteed. FIFO request queueing, priority queueing, and priority queueing with preemptable service are simulated for a range of CPU computati ...

14 Cache Memories

Alan Jay Smith
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
Publisher: ACM Press

Full text available: pdf(4.61 MB) Additional Information: full citation, references, citings, index terms

15 Resource partitioning in general purpose operating systems: experimental results in Windows NT

D. G. Waddington, D. Hutchison

October 1999 **ACM SIGOPS Operating Systems Review**, Volume 33 Issue 4

Publisher: ACM Press

Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, index terms

The principal role of the operating system is that of resource management. Its task is to present a set of appropriate services to the applications and users it supports. Traditionally, general-purpose operating systems, including Windows NT, federate resource sharing in a fair manner, with the predominant goal of efficient resource utilisation. As a result the chosen scheduling algorithms are not suited to applications that have stringent Quality-of-Service (QoS) and resource management require ...

16 Fairisle: an ATM network for the local area

Ian Leslie, Derek McAuley

August 1991 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Communications architecture & protocols SIGCOMM '91**, Volume 21 Issue 4

Publisher: ACM Press

Full text available: pdf(773.54 KB) Additional Information: full citation, references, citings, index terms

17 A simple and efficient bus management scheme that supports continuous streams

Saied Hosseini-Khayat, Andreas D. Bovopoulos

May 1995 **ACM Transactions on Computer Systems (TOCS)**, Volume 13 Issue 2

Publisher: ACM Press

Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings, index terms, review

An efficient bandwidth management and access arbitration scheme for an I/O bus in a multimedia workstation is presented. It assumes that a multimedia workstation consists of a number of processing modules which are interconnected by a packet bus. The scheme is efficient in the sense that it allows the bus to support both continuous media transfers and regular random transactions in such a way that continuous streams can meet their real-time constraints independently of random traffic, and r ...

Keywords: bus arbitration, bus management, continuous stream, multimedia workstation

18 Monitor classification

Peter A. Buhr, Michel Fortier, Michael H. Coffin

March 1995 **ACM Computing Surveys (CSUR)**, Volume 27 Issue 1

Publisher: ACM Press

Full text available: pdf(3.41 MB) Additional Information: full citation, abstract, references, citings, index terms

One of the most natural, elegant, and efficient mechanisms for synchronization and communication, especially for systems with shared memory, is the monitor. Over the past twenty years many kinds of monitors have been proposed and implemented, and many modern programming languages provide some form of monitor for concurrency control. This paper presents a taxonomy of monitors that encompasses all the extant monitors and suggests others not found in the literature or in exist ...

Keywords: classification, monitors

19 Multicast contention resolution with single-cycle windowing using content addressable FIFO's

Kenneth J. Schultz, P. Glenn Gulak
October 1996 **IEEE/ACM Transactions on Networking (TON)**, Volume 4 Issue 5
Publisher: IEEE Press
Full text available: pdf(1.12 MB) Additional Information: full citation, references, index terms

20 Third Generation Computer Systems

Peter J. Denning
December 1971 **ACM Computing Surveys (CSUR)**, Volume 3 Issue 4
Publisher: ACM Press
Full text available: pdf(3.52 MB) Additional Information: full citation, abstract, references, citings, index terms

The common features of third generation operating systems are surveyed from a general view, with emphasis on the common abstractions that constitute at least the basis for a "theory" of operating systems. Properties of specific systems are not discussed except where examples are useful. The technical aspects of issues and concepts are stressed, the nontechnical aspects mentioned only briefly. A perfunctory knowledge of third generation systems is presumed.

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